## REMARKS

In the Office Action dated June 4, 2001, claims 1-6 were presented for examination. The Examiner rejected claims 2-6 under 35 U.S.C. §112, second paragraph, and claims 1-6 under 35 U.S.C. §103(a).

Applicant wishes to thank the Examiner for the careful and thorough review and action on the merits in this application. The following remarks are provided in support of the pending claims and responsive to the Office Action of June 4, 2001 and Advisory Action of November 21, 2001 for the pending application.

### I. Rejection of Claims 2-6 under 35 U.S.C. §112, second paragraph

In the Office Action of June 4, 2001, the Examiner assigned to the application rejected the claims as containing omissions between the elements. The Examiner raised the issue as to whether the "memory" in line 17 of claim 1 is the same as "physical memory". More specifically, the Examiner raised issue in claim 2 in that the relationship between the "physical memory" element and "data structure" element is not clear. Applicant has amended claim 1, as shown, to clarify the identification of the term memory as noted by the Examiner. In addition, Applicant has amended claim 2 to clarify the relationship between the "physical memory" element and the "data structure" element. Additionally, claim 2 has been amended to clarify that the data structure is stored in memory on each node. Finally, the Examiner raised an issue in claim 3 as to the data structures, and more specifically that they may be different data structures. Applicant has added new claims 7-10 to further clarify this aspect. Since the amendment to the claims was not entered or considered in response to the Office Action of June 4, 2001, Applicant respectfully requests the Examiner to enter the amendment submitted herewith in conjunction with the Request for Continued Examination filed herewith.

### II. Rejection of claims 1-6 under 35 U.S.C. §103(a)

Claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Slingwine et al.*(U.S. Patent No. 5,727,209) in view of *Roche et al.* (U.S. Patent No. 4,916,697).

As noted by the Examiner, *Slingwine et al.* teaches a multiprocessor computer system having interconnected nodes. "A summary of thread activity tracks which threads have passed through a quiescent state after the current generation of updates was started. When the last thread related to the current generation passes through a quiescent state, the summary of thread activity signals a callback processor that it is safe to end the current generation of updates." Abstract, lines 11-17. However, as noted by the Examiner *Slingwine et al.* does not teach or suggest use of a bit mask to indicate whether a processor has passed through a quiescent state. See Second Office Action, page 4. Accordingly, as noted by the Examiner, *Slingwine et al.* fails to teach or suggest all of the limitations as claimed by Applicant.

The *Roche et al.* patent is cited by the Examiner to support the use of a bit mask to record a thread passing through a quiescent state. However, *Roche et al.* pertains to error detection and classification of the error. For example, an L1error is generated in response to concurrently stopping a multiple unit partition, an L2 error causes only the detecting unit to stop as soon as possible, and an L3 error does not require any clock intervention anywhere in the processor. Accordingly, *Roche et al.* discloses use of a bit mask to classify errors, but it does not teach or suggest use of a bit mask to indicate whether a processor has passed through a quiescent state.

Applicant's invention as shown in claims 1-10 functions on a different principle than that taught in the combination of *Slingwine al.* and *Roche et al.* As per Applicant's claim 1, there is a first level bit mask and a second level bit mask. The first level bit mask contains "a bit per node, the bit indicating whether the corresponding node contains a processor that has not yet passed through a quiescent state." The second level bit mask contains "a bit per processor associated with a particular node . . . the bit indicating whether the corresponding processor has not yet passed through a quiescent state." As noted by the Examiner, *Slingwine et al.* fails to teach a level bit mask as an indication of passing through a quiescent state. Although *Roche et al.* teaches the use of bit masks in a multiprocessing system, the bit masks of *Roche et al.* are limited to classification of errors and does not suggest applying the bit mask to indicate whether a processor has passed through a quiescent state. Applicant's invention, as supported in the language of the claims, includes the use of a first level bit mask and a second level bit mask, both

pertaining to indicating passing of a corresponding processor through a quiescent state. The use by Applicant of two or more bit mask levels mitigates the number of remote accesses for each processor in a multiple node computer system.

As per claim 2, Applicant requires "a data structure stored in the physical memory on each node for storing a number of the current generation of data elements being processed by a processor on a node." In addition, Applicant has further amended claim 2 to include "wherein the current generation number on the nodes are updated in lockstep so that the nodes have local access to copies of the current generation number." Neither *Slingwine et al.* nor *Roche et al.* teaches or suggests storing a current generation number on each node nor updating the current generation numbers in lockstep. Accordingly, there is no support or motivation for *Slingwine et al.* or *Roche et al.* to update the current generation number in the manner taught by Applicant.

As per claim 3, Applicant requires a first data structure on a processor's node, a second data structure on a processor's node, and a third data structure accessible to all the nodes. Neither *Slingwine et al.* nor *Roche et al.* teaches or suggests the distribution or functionality of data structures as taught by Applicant. As such, there is no support or motivation for *Slingwine et al.* or *Roche et al.* to implement the distribution and functionality of the data structures of Applicant to determine if a processor has passed through a quiescent state.

For it to be obvious to combine prior art references, the references must teach, suggest, or motivate one with ordinary skill in the art to combine the references and create the claimed invention. "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." MPEP §2143.01. Neither the *Slingwine et al.* or *Roche et al.* patents support the use of a bit mask to indicate wither a corresponding processor has passed through a quiescent state. Furthermore, neither *Slingwine et al.* or *Roche et al.* teach the use of bit masks or multiple data structures to indicate whether a corresponding processor has passed through a quiescent state. Accordingly, neither *Slingwine et*

*al.* nor *Roche et al.* teach or suggest the use of two or more bit masks or two or more data structures to indicate whether an associated processor has passed through a quiescent state.

In fact, both *Slingwine et al.* and *Roche et al.* fail to address Applicant's use and placement of bit masks and/or data structures. "Although a prior art device may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." MPEP §2143.01 (citing *In re Mills*, 916 F.2d 680, 682, 16 USPQ 2d. 1430 (Fed. Cir. 1990)). *Slingwine et al.* does not suggest use of a bit mask and/or data structures as taught by Applicant, and *Roche et al.* does not suggest modifying the use and/or placement of their bit mask and/or data structures to meet the placement and functionality of Applicant's bit mask and/or data structures. To read *Roche et al.* as providing the structure that supports use of a bit mask to indicate whether an associated processor has passed through a quiescent state would require a modification to the invention of *Roche et al.* not envisioned or taught. The only suggestion for a system that utilizes two or more bit masks and/or data structures that supports an indication as to whether an associated processor has passed through a quiescent state is derived from Applicant's invention. Absent Applicant's invention, there is no suggestion or motivation within the combination of *Slingwine et al.* and *Roche et al.* for such a modification. "It is impermissible to use the claimed invention as an instructions manual or 'template' to piece togther the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ 2d 1780 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991)). Yet this is the very process that the Examiner has attempted to undertake. Accordingly, the combination of the prior art references is improper as the Examiner's combination is precipitated by utilizing Applicant's claimed invention as the template to make the modifications suggested by the Examiner – which by its very nature makes such a combination non-obvious.

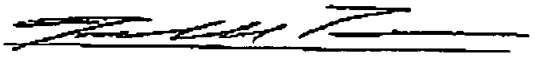
The teaching, suggestion, or motivation for combining the references must emanate from the references themselves, and not from Applicant. The prior art must teach the desirability of the modification in question. "The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the

modification." *In re Gordon et al.*, 733 F.2d 900, 221 USPQ 1125, 1127 (Fed. Cir. 1984). There is no desire within the references themselves to combine the elements of the prior art to arrive at Applicant's invention. The desirability can be found at best only through the use of Applicant's invention. Therefore, the prior art references whether taken individually or in combination do not render Applicant's invention obvious as there is no teaching, suggestion, or motivation to combine the elements found in different prior art references having different purposes to build the product of Application. Accordingly, Applicants respectfully contend that the combination of *Slingwine et al.* and *Roche et al.* does not meet the standard set by the CAFC's interpretation of 35 U.S.C. §103(a), and respectfully requests allowance of claims 1-10.

In view of the forgoing remarks it is submitted that all of the claims remaining in the application are now in condition for allowance and such action is respectfully requested. Should any questions arise in connection with this application or should the Examiner believe that a telephone conference with the undersigned would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that she be contacted at the number indicated below.

For the reasons outlined above, an allowance of this application are respectfully requested.

Respectfully submitted,

By: 

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